REMARKS

Applicants respectfully request favorable reconsideration of the subject application, as amended.

Initially, Applicants note that the Form PTOL-326 accompanying the Office Action indicates that the drawings are objected to. However, no objection to the drawings is apparent in the Office Action. Thus, Applicants presume that the drawings submitted January 3, 2007, are acceptable. Confirmation in the next Office communication is respectfully requested.

By this Amendment, Claims 48, 49, 55, 58 and 70-72 have been amended to more particularly recite subject matter Applicants' regard as their invention and to address the informalities alleged in items 6 and 7 of the Office Action, as discussed in detail below. Claims 1-47 were previously cancelled without prejudice or disclaimer. Thus, Claims 48-72 are pending.

In the Office Action, Claims 48-72 were rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter; Claims 55-70 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly being not enabled; Claims 48-72 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite; Claims 48-72 were rejected under 35 U.S.C. § 102(e) over Killian et al. ("Killian"); and Claims 48-72 were rejected under 35 U.S.C. § 102(e) over Lin et al. ("Lin").

Rejections Under 35 U.S.C. § 112

Without acceding to the rejection under 35 U.S.C. § 112, first paragraph, Applicants have amended Claim 55 to recite, *inter alia*, a data processing system in

place of the term "data processing means" cited in the rejection. Support for the amendment is provided, for example, at paragraphs [0096] and [0230] of Applicants' published application Pub. No. 2004/0158788 ("the published application").

Applicants respectfully submit that Claims 55-70 are sufficiently enabled by Applicants' specification at, for example, the portions of the published application cited above. Applicants respectfully request that this rejection be withdrawn.

Further, without acceding to the rejections under 35 U.S.C. § 112, second paragraph, Applicants have amended the Claims to more particularly recite subject matter which Applicants' regard as their invention.

For example, regarding item 7(ii) in the Office Action, Claims 48 and 71 have been amended to recite, *inter alia*, receiving in memory functional specification data obtained by replacing, at least by a language adaptation device, the software model that physically describes the ASIC comprising a circuit under design to be validated. Support is provided, for example, at para. [0053] of the published application.

Regarding item 7(iii) in the Office Action, Claims 48 and 71 have been amended to recite, *inter alia*, an autonomous circuit emulator built around a data processing system, in place of the "constituted" term. Support is provided, for example, at para. [0096] of the published application.

Regarding item 7(iv) in the Office Action, Claims 48 and 71 have been amended to recite, *inter alia*, when the response data of the software model are not identical to the response data structures. Support is provided, for example, at paragraphs [0115], [0117] and [0118] of the published application.

Regarding item 7(v) in the Office Action, Claims 48 and 71 have been amended to recite, *inter alia*, utilizing the verification platform in the verification

mode, by comparing response data from interfaces of the software model with the response data structures taken as a reference for the validation of response data transmitted by the software model. Support is provided, for example, at paragraphs [0115], [0117] and [0118] of the published application.

Regarding item 7(vi) in the Office Action, Claims 48 and 71 have been amended to recite, *inter alia*, an autonomous circuit emulator built around a data processing system, receiving in memory functional specification data obtained by replacing, at least by a language adaptation device, the software model that physically describes the ASIC comprising a circuit under design to be validated, with a high level language abstract description, the autonomous circuit emulator generating response data structures in accordance with said functional specification data, as a function of stimuli received from an environment emulator. Support is provided, for example, at para. [0096] of the published application.

Regarding item 7(vii) in the Office Action, Claims 49 and 72 have been amended to recite, *inter alia*, comparing output stimuli of both the response data of the software model of the ASIC and the response data structures. Support is provided, for example, at para. [0118] of the published application.

Regarding item 7(viii) in the Office Action, regarding the clarification of the term "validating the software model" contained in Claims 49 and 72, Claims 48 and 71 from which Claims 49 and 72 respectively depend have been amended to recite, *inter alia*, validating the software model or invalidating the software model by outputting one or more error notifications when the response data of the software model are not identical to the response data structures. Support is provided, for example, at paragraphs [0115], [0117] and [0118] of the published application.

Regarding item 7(ix) in the Office Action, Claim 55 has been amended to recite, *inter alia*, a data processing system receiving selection requests from a client to select test models producing input stimuli applied to the software model of the ASIC, said data processing system comprising in memory functional specification elements of the ASIC which are read in a high level language and comprising in memory a sequence of programmed instructions of an emulator program that generates output stimuli of a functional validation test program. Support is provided, for example, at paragraphs [0096], [0113], [0114] and [0230] of the published application.

Regarding item 7(x) in the Office Action, Applicants respectfully submit that the recitations of Claims 62 and 63 directed to functions for which the emulator is configured are sufficiently definite to particularly point out and distinctly claim subject matter which Applicants regard as their invention. In particular, incorrect prediction readjustment is described, for example, at paragraphs [0207], [0208] and [0209] of the published application. Furthermore, reducing the number of valid hypotheses is described, for example, at paragraphs [0210] to [0214], and collision termination is described, for example, at paragraphs [0215] to [0217].

Regarding item 7(xi) in the Office Action, Claim 55 has been amended to recite, *inter alia*, generation of predictions is performed by the emulator of the circuit after receiving information on the internal operation of the circuit. Support is provided, for example, at paragraphs [0137] to [0139] and [0204] of the published application.

In view of the foregoing, Applicants respectfully submit that Claims 48-72 are set forth with sufficient definiteness as to particularly point out and distinctly claim

subject matter which Applicants regard as their invention. Applicants respectfully request that this rejection be withdrawn.

The objection to the claims at page 6 of the Office Action is not understood. However, Applicants respectfully submit that any objections to the claims are overcome by the amendments to the claims addressing the rejections under 35 U.S.C. § 112 as discussed above. Withdrawal of the objection to the claims is respectfully requested.

Accordingly, Applicants respectfully request that the rejections under 35 U.S.C. § 112 be withdrawn.

Rejection Under 35 U.S.C. § 101

Without acceding to the rejection under 35 U.S.C. § 101, Claims 48 and 71 as amended recite, *inter alia*, comparing response data from interfaces of the software model with the response data structures taken as a reference for the validation of response data transmitted by the software model, and validating the software model or invalidating the software model by outputting one or more error notifications when the response data of the software model are not identical to the response data structures. Support is provided, for example, at paragraphs [0115], [0117] and [0118] of Applicants' published application.

Therefore, Applicants respectfully submit that Claims 48 and 71 are not directed to mere manipulation of an abstract idea but instead produce a useful, tangible and concrete result; for example, the outputting of one or more error notifications when the response data of the software model are not identical to the

response data structures, in accord with *State Street Bank & Trust Co. v. Signature Financial Group Inc.*, 149 F.3d 1368 (Fed. Cir. 1998).

Further, Claim 55 as amended recites, *inter alia*, that a comparator compares the output stimuli of the functional validation test program with output stimuli of the software model and that one or more error notifications are output when compared output stimuli are not identical. Support is provided, for example, at paragraphs [0115], [0117] and [0118] of Applicants' published application.

Thus, Applicants believe that Claim 55 is also directed to patent eligible subject matter for at least the reasons discussed above with respect to Claims 48 and 71.

In addition, Claims 48 and 71 as amended now recite, *inter alia*, an environment emulator debug mode. Support is provided at, for example, paragraph [0105] of Applicants' published application. It is clear that the environment emulator debug mode recited in Claims 48 and 71 does not read on a signal.

Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 101 be withdrawn.

Rejections Under 35 U.S.C. § 102

Turning to the merits, Claims 48-72 were rejected under 35 U.S.C. § 102(e) over Killian and Lin.

Without acceding to the rejections under 35 U.S.C. § 102, Claims 48, 55 and 71 have been amended to more particularly recite subject matter Applicants' regard as their invention.

In particular, Claims 48 and 71 have been amended to recite, *inter alia*, creating, in the environment emulator debug mode, an autonomous circuit emulator built around a data processing system, receiving in memory functional specification data obtained by replacing, at least by a language adaptation device, the software model that physically describes the ASIC comprising a circuit under design to be validated, with a high level language abstract description, and that the autonomous circuit emulator generates response data structures in accordance with functional specification data, as a function of stimuli received from an environment emulator. Support is provided, for example, at paragraph [0096] of Applicants' published application. It is apparent that Killian and Lin do not teach or suggest at least the above-discussed features of Claims 48 and 71.

For example, Killian, in contrast with Claims 48 and 71, teaches an emulation board that uses a complex programmable logic device to emulate, in hardware, a processor configuration. *See* Killian, col. 32, lines 11-24; and FIG. 6. Killian's complex programmable logic device is programmed with the processor netlist. *Id.* Thus, it is apparent that Killian does not teach or suggest creating . . . an autonomous circuit emulator built around a data processing system, receiving in memory functional specification data obtained by replacing, at least by a language adaptation device, the software model that physically describes the ASIC comprising a circuit under design to be validated, and that the autonomous circuit emulator generates response data structures in accordance with functional specification data, as recited in Claims 48 and 71.

Further, Lin, in contrast with Claims 48 and 71, teaches a simulation/verification system that contains the hardware model of the user design

and which contains an array of reconfigurable logic elements. *See* Lin, col. 16, lines 52-54. Lin also teaches that a programmer uses files along with hardware programmable devices to program an FPGA array. Lin, col. 40, lines 51-53. Thus, it is apparent that Lin does not teach or suggest creating . . . an autonomous circuit emulator built around a data processing system, receiving in memory functional specification data obtained by replacing, at least by a language adaptation device, the software model that physically describes the ASIC comprising a circuit under design to be validated, with a high level language abstract description, as recited in Claims 48 and 71.

Therefore, Applicants respectfully submit that Claims 48 and 71 distinguish patentably from the applied references.

Furthermore, Claim 55 has been amended to recite, *inter alia*, a data processing system receiving selection requests from a client to select test models producing input stimuli applied to the software model of the ASIC, the data processing system comprising in memory functional specification elements of the ASIC which are read in a high level language and comprising in memory a sequence of programmed instructions of an emulator program that generates output stimuli of a functional validation test program, in relation to the input stimuli and the functional specification elements. Support is provided, for example, at paragraphs [0096] and [0230] to [0232] of Applicants' published application. It is apparent that Killian and Lin do not teach or suggest at least the above-discussed features of Claim 55.

For example, Killian, in contrast with Claim 55, teaches an emulation board that uses a complex programmable logic device to emulate, in hardware, a processor configuration. *See* Killian, col. 32, lines 11-24; and FIG. 6. Killian's complex

programmable logic device is programmed with the processor netlist. *Id.* Thus, it is apparent that Killian does not teach or suggest a data processing system receiving selection requests from a client to select test models producing input stimuli applied to the software model of the ASIC, as recited in Claim 55.

Claim 55 also recites, *inter alia*, a data processing system comprising in memory functional specification elements of the ASIC which are read in a high level language and comprising in memory a sequence of programmed instructions of an emulator program that generates output stimuli of a functional validation test program, in relation to the input stimuli and the functional specification elements.

Lin, in contrast with Claim 55, teaches a simulation/verification system that contains the hardware model of the user design and which contains an array of reconfigurable logic elements. *See* Lin, col. 16, lines 52-54. Lin also teaches that a programmer uses files along with hardware programmable devices to program an FPGA array. Lin, col. 40, lines 51-53. Thus, it is apparent that Lin does not teach or suggest a data processing system comprising in memory functional specification elements of the ASIC which are read in a high level language and comprising in memory a sequence of programmed instructions of an emulator program that generates output stimuli of a functional validation test program, in relation to the input stimuli and the functional specification elements, as recited in Claim 55.

Therefore, Applicants respectfully submit that Claim 55 distinguishes patentably from the applied references.

The remaining claims are also believed to be patentable at least due to their dependence from Claims 48, 55 and 71 as well as for the additional features recited in the remaining claims.

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. A prompt Notice of Allowance is respectfully requested.

Should the Examiner believe that any further action is necessary to place this application in better form for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T2147-908627) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

MILES & STOCKBRIDGE, P.C.

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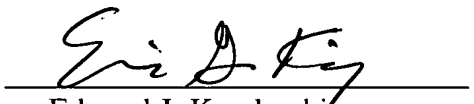
By: 

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